REMARKS

Applicants acknowledge the allowance of claims 17-32 and 54-67 and the indication of allowability of claims 3, 11-16, and 46-53. In relation to the stated reasons for allowance (Paper 9 at 9), Applicants agree with the reasoning, in general. However, Applicants believe that other bases for patentability exist as well in limitations and combinations of limitations not commented upon in the Office Action. Claims 1, 33-37, 40, 41, and 42 are amended. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment.

Claim 37 stands objected to as containing an incorrectly spelled word. The amendment to claim 37 should overcome this objection and it is respectfully requested to be withdrawn.

Claims 33-41 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicants respectfully traverse this rejection. In view of the clarifying amendment to claims 33-36, 40, and 41, the rejection under section 112, second paragraph, is now overcome.

Claims 1, 2, 4-6, 33, 34, 40, and 41 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. patent 6,097,070 (Mandelman et al.). Applicants respectfully traverse this rejection.

Claim 1, as amended, defines a semiconductor device and recites: "a substrate having at least two spaced doped source/drain regions, said source/drain regions defining a channel region therebetween" and "a transistor gate over said substrate and wholly between said spaced doped source/drain regions, said transistor gate having one first gate electrode of a first conductivity type and two second gate electrodes of a second conductivity type, wherein said two second gate electrodes are provided on either side of said first gate electrode and are separated from said first gate electrode by an insulating dielectric layer." Mandelman et al. does not disclose such a device.

Mandelman et al. at least does not disclose "a transistor gate over said substrate and wholly between said spaced doped source/drain regions." Mandelman et al. discloses just the opposite, that "outer gate conductors are above a portion of the source and drain regions." See column 1, lines 61-62; column 3, lines 7 and 14; and FIG. 2. This overlap shortens the channel (20) length of the Mandelman et al. transistor and would not serve to mitigate short channel effects.

Since Mandelman et al. does not disclose each limitation of claim 1, this independent claim is not anticipated by the reference. Claims 2-16, depending from claim 1, are likewise patentable over Mandelman et al. Applicants respectfully request that the 35 U.S.C. § 102(e) rejection of claims 1, 2, and 4-6 be withdrawn.

Claim 33, as amended, defines a semiconductor device and recites, in part, "three gate electrodes over said substrate and at least partially between said source/drain regions, including a center gate electrode of P+ type conductivity and two adjacent outer gate electrodes of N+ type conductivity" and "a first conductive cap layer over said center gate electrode and a second conductive cap layer electrically connecting said outer gate electrodes." Mandelman et al. does not anticipate this claimed device.

Mandelman et al. at least does not disclose the three gate electrodes and the first and second conductive cap layers associated with those electrodes recited in claim 33. Mandelman et al. discloses only the single gate cap (24) electrically connecting all three electrodes together. Column 3, line 2; column 4, line 63; FIG. 2.

Since Mandelman et al. does not disclose each and every limitation of independent claim 33, neither this nor any claim depending therefrom (i.e., claims 34-41) is anticipated by the reference. Applicants respectfully request that the 35 U.S.C. § 102(e) rejection of claims 33, 34, 40, and 41 be withdrawn.

Claims 42-45 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. patent 6,348,387 (Yu). Applicants respectfully traverse this rejection.

Claim 42, as amended, defines a transistor structure and recites, in part, "a gate dielectric over said substrate" and "a central gate electrode over said channel region and said gate dielectric" and "two outer gate electrodes over said channel region and said gate dielectric and adjacent to said central gate electrode, said outer gate electrodes being separated from said central gate electrode by a dielectric layer, and wherein said gate dielectric where under said two outer gate electrodes is equal in thickness to or thinner than said gate dielectric where under said central gate electrode." Yu does not anticipate this claimed device.

Yu at least does not disclose a "gate dielectric where under said two outer gate electrodes is equal in thickness to or thinner than said gate dielectric where under said central gate electrode." In fact, Yu discloses the opposite, that its gate dielectric layer (208 and 212) is 15 Å to 25 Å thick and the liner dielectric (218) is 50 Å to 80 Å thick. Column 3, lines 48-50; column 4, lines 22, 47-54; and FIGs. 2-5.

Since Yu does not disclose each and every limitation of independent claim 44, this claim and each dependent claim, i.e., claims 43-53, is patentable over this reference. Applicants respectfully request that the 35 U.S.C. § 102(e) rejection of claims 42-45 be withdrawn.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Mandelman et al. in view of U.S. patent 5,356,821 (Naruse et al.) Applicants respectfully traverse this rejection.

Claim 7 depends from claim 1, which as discussed above, is patentable over Mandelman et al. Naruse et al. adds no teaching or suggestion to the disclosure of Mandelman et al. so as to have rendered the subject matter of claim 7 obvious. In particular, Naruse et al. at least does not teach or suggest a three-electrode transistor gate over said substrate and wholly between said spaced doped source/drain regions. Naruse et al. cannot overcome the deficiencies in the disclosure of Mandelman et al. in relation to

claim 1 so as to have rendered its subject matter obvious. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claim 7 be withdrawn.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Mandelman et al. in view of U.S. patent 5,886,368 (Forbes et al.) Applicants respectfully traverse this rejection.

Claim 8 depends from claim 1, which as discussed above, is patentable over Mandelman et al. Forbes et al. adds no teaching or suggestion to the disclosure of Mandelman et al. so as to have rendered the subject matter of claim 8 obvious. In particular, Forbes et al. at least does not teach or suggest a three-electrode transistor gate over said substrate and wholly between said spaced doped source/drain regions. Forbes et al. cannot overcome the deficiencies in the disclosure of Mandelman et al. in relation to claim 1 so as to have rendered its subject matter obvious. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claim 8 be withdrawn.

Claims 9 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mandelman et al. in view of U.S. patent 6,274,510 (Wilk et al.). Applicants respectfully traverse this rejection.

Claims 9 and 10 depend from claim 1, which as discussed above, is patentable over Mandelman et al. Wilk et al. adds no teaching or suggestion to the disclosure of Mandelman et al. so as to have rendered the subject matter of claims 9 and 10 obvious. In particular, Wilk et al. at least does not teach or suggest a three-electrode transistor gate over said substrate and wholly between said spaced doped source/drain regions. Wilk et al. cannot overcome the deficiencies in the disclosure of Mandelman et al. in relation to claim 1 so as to have rendered its subject matter obvious. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 9 and 10 be withdrawn.

Claim 35 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Mandelman et al. in view of Naruse et al. Applicants respectfully traverse this rejection.

Claim 35 depends from claim 33, which as discussed above, is patentable over Mandelman et al. Naruse et al. adds no teaching or suggestion to the disclosure of Mandelman et al. so as to have rendered the subject matter of claim 35 obvious. In particular, Naruse et al. at least does not teach or suggest the three gate electrodes and the first and second conductive cap layers associated with those electrodes recited in claim 33. Naruse et al. cannot overcome the deficiencies in the disclosure of Mandelman et al. in relation to claim 33 so as to have rendered its subject matter obvious. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claim 35 be withdrawn.

Claim 36 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Mandelman et al. in view of Forbes et al. Applicants respectfully traverse this rejection.

Claim 36 depends from claim 33, which as discussed above, is patentable over Mandelman et al. Forbes et al. adds no teaching or suggestion to the disclosure of Mandelman et al. so as to have rendered the subject matter of claim 36 obvious. In particular, Forbes et al. at least does not teach or suggest the three gate electrodes and the first and second conductive cap layers associated with those electrodes recited in claim 33. Forbes et al. cannot overcome the deficiencies in the disclosure of Mandelman et al. in relation to claim 33 so as to have rendered its subject matter obvious. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claim 36 be withdrawn.

Claims 37 and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mandelman et al. in view of Wilk et al. Applicants respectfully traverse this rejection.

Claims 37 and 38 depend from claim 33, which as discussed above, is patentable over Mandelman et al. Wilk et al. adds no teaching or suggestion to the disclosure of Mandelman et al. so as to have rendered the subject matter of claims 37 and 38 obvious. In particular, Wilk et al. at least does not teach or suggest the three gate electrodes and the first and second conductive cap layers associated with those electrodes recited in claim 33. Wilk et al. cannot overcome the deficiencies in the disclosure of Mandelman et al. in

relation to claim 33 so as to have rendered its subject matter obvious. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 37 and 38 be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By /MJT/ #33,082

Mark J. Thronson
Registration No.: 33,082
Ryan H. Flax
Registration No.: 48,141
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicants

Version With Markings to Show Changes Made

1. (Amended) A semiconductor device comprising:

a substrate having at least two spaced doped source/drain regions, said source/drain regions defining a channel region therebetween; and

a transistor gate over said substrate and wholly between said spaced doped source/drain regions, said transistor gate having one first gate electrode of a first conductivity type and two second gate electrodes of a second conductivity type, wherein said two second gate electrodes are provided on either side of said first gate electrode [,] and are separated from said first gate electrode by an insulating dielectric layer.

33. (Amended) A semiconductor device, comprising:

a semiconductor substrate, said substrate having at least two separated doped source/drain regions;

three gate electrodes over said substrate and at least partially between said source/drain regions, including a center gate electrode of P+ type conductivity and two adjacent outer gate electrodes of N+ type conductivity;

a gate dielectric separating said three gate electrodes from said substrate;

a thin dielectric layer separating said outer gate electrodes from said center gate electrode;

a first conductive cap layer over said [three vertical] center gate electrode[s, said] and a second conductive cap layer electrically connecting said [three vertical] outer gate electrodes; and

insulating sidewalls adjacent to said conductive cap layer and said outer gate electrodes.

34. (Amended) The semiconductor device of claim 33, wherein the three [vertical] gate electrodes comprise doped polysilicon.

35. (Amended) The semiconductor device of claim 33, wherein the [central] center gate electrode comprises silicon-germanium.

36. (Amended) The semiconductor device of claim 33, wherein the three [vertical] gate electrodes comprise a material selected from the group consisting of silicon-carbide and silicon oxycarbide.

37. (Amended) The semiconductor device of claim 33, wherein the dielectric layer comprises a material selected from the group consisting of nitride, oxynitride, and nitrided [oxyide] oxide.

40. (Amended) The semiconductor device of claim 33, wherein a workfunction difference exists between the [central] center gate electrode and the outer gate electrodes.

41. (Amended) The semiconductor device of claim 40, wherein said workfunction difference results in the [central] center gate electrode having a higher threshold voltage than said outer gate electrodes.

42. (Amended) A transistor structure comprising:

a semiconductor substrate having at least two spaced doped source/drain regions, said source/drain regions defining a channel region therebetween;

a gate dielectric over said substrate;

a central gate electrode over said channel region and said gate dielectric; and

two outer gate electrodes over said channel region and said gate dielectric and adjacent to said central gate electrode, said outer gate electrodes being separated from said central gate electrode by a dielectric layer, and wherein said gate dielectric where under said

two outer gate electrodes is equal in thickness to or thinner than said gate dielectric where under said central gate electrode;

wherein a workfunction difference between the central gate electrode and the outer gate electrodes is such that said central gate electrode experiences a greater threshold voltage than said outer gate electrodes.